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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,714	08/13/2001	Andreas Falkenberg	2001P14844US	8927

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Siemens Corporation
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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/929,714	FALKENBERG, ANDREAS	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Applicant Arguments or Remarks03/14/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2005* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The modifications to the drawings were received on 03/14/2005. These modifications are accepted by the Examiner.

Specification

The modifications to the specification were received on 03/14/2005. These modifications are accepted by the Examiner.

Response to Arguments

Applicant's arguments filed on 03/14/2005 have been fully considered but they are not persuasive.

As per claim 21:

The Applicant contends, "Kosaka1 does not teach or suggest mapping the translated bits to DQPSK symbols where each DQPSK symbol is represented by a single in-phase component and a single quadrature phase component, as required by amended Claim 21. For at least the foregoing reasons, Kosaka1 fails to disclose, suggest, or teach Applicant's claimed invention ms recited in Claim 21.".

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, Kosaka (US5369378) discloses mapping the translated bits to DQPSK symbols where each DQPSK symbol is represented by a single in-phase component (I0I1) and a single quadrature phase component (Q0Q1) (figure 9 column 6 line 65 column 7 line 11 and column 7 lines 52-60). The Applicant's representative expressively agrees indicating that statement: "Kosaka1 discloses obtaining two communication bits YK and

XK (Col. 6, lines 51-52) and using the two communication bits and the preceding symbol to translate the two communication bits into a 3-bit output SM0, SMI and SM2 (See Col. 6, lines 58-61., Figure 8; Col. 6, line 47,. Figure 8., Col. 8, line 68, Col. 7, lines 1-1 1; Figure 9). The translation technique described in Kosaka1 maps the 3-bit output SM0, SMI and SM2 to symbol mapping data I0, I1, Q0 and Q1. The Kosaka1 process maps to 2-bits for the I phase (10 and 11) and 2-bits for the Q phase (Q0 and Q1). (Col. 7, lines 52-68; Col. 8, lines 1-3.)". For these reasons and the reason stated en the previous Office Action, the rejection of claim 21 is maintained.

As per claim 22:

The Applicant contends, "Kosaka2 fails to disclose or suggest "obtaining Pi/4 demodulation quadrature phase shift keying (DQPSK) symbols," recited in Claim 22. Kosaka2 also fails to disclose or suggest "translating the Pi/4 DQPSK symbols into quadrature phase shift keying (QPSK) symbols," recited in Claim 22."

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, Kosaka (US 5355092) discloses obtaining Pi/4 demodulation quadrature phase shift keying (DQPSK) symbols, and translating the Pi/4 DQPSK symbols into quadrature phase shift keying (QPSK) symbols (figures 1-7 column 2 line 61 to column 6 line 3 figures 4 and 6 column 3). For these reasons and the reason stated en the previous Office Action, the rejection of claim 22 is maintained.

As per claims 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17 and 20

The Applicant contends that, "Kosaka2 fails to disclose or suggest "obtaining Pi/4 demodulation quadrature phase shift keying (DQPSK) symbols," recited in Claim 22.

Kosaka2 also fails to disclose or suggest translating the Pi/4 DQPSK symbols into quadrature phase shift keying (QPSK) symbols. Kosaka2 does not disclose, suggest or teach: a storage device . . . having . . . information for covering the processing unit to: obtain Pi/4 differential quadrature phase shift keying (DQPSK) symbols; translate the Pi/4 DQPSK symbols into quadrature phase shift keying (QPSK) symbols recited in Claim 10; nor does it disclose, suggest or teach: means for obtaining Pi/4 differential quadrature phase shift keying (DQPSK) symbols; translating the Pi/4 DQPSK symbols into quadrature phase shift keying (QPSK) symbols"

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, Kosaka (US 5355092) discloses obtaining Pi/4 demodulation quadrature phase shift keying (DQPSK) symbols, and translating the Pi/4 DQPSK symbols into quadrature phase shift keying (QPSK) symbols (figures 1-7 column 2 line 61 to column 6 line 3 figures 4 and 6 column 3). For these reasons and the reason stated en the previous Office Action, the rejection of claims 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17 and 20 is maintained.

As per claims 3, 4, 13, 18, and 19.

The Applicant contends again that, "Kosaka2 teaches that "in order to demodulate the (Pi/4) ... shift QPSK modulated signal .. . (according to the equation referred to by the Examiner), at each maximal effect point, the phase ... at the symbol and the phase . .. at an immediately preceding symbol are detected."

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, Kosaka (US 5355092) discloses phase change calculation for demodulation

(Kosaka2 column 3 lines 43-65). Dutta (US 5313493) discloses using the formulas s'(t)=m(t)m(t-T)exp[j{Δwt-Δw(t-T)}]. Letting s'(t) =SQPSK (t), m(t) =S9T) and T=1 this formula can be equated to the formula clamed by Applicant in claims 3, 13 and 18 (Dutta column 6 lines 35-60). AS to claims 4 and 19 the formula disclosed by Dutta can be applied to the disclosed by Kosaka2 Petersen (US 2001/0031024) discloses a demodulation translating Pi/4 DQPSK symbols into QPSK symbols (Petersen paragraphs [0004] to [0008] and table 1]. For these reasons and the reason stated en the previous Office Action, the rejection of claims 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17 and 20 is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Kosaka (US 5369378) (hereto referred to as Kosaka1). Kosaka1 discloses a method for modulation of a communication signal, using Differential quadrature phase shift keying (DQPSK). Kosaka1 teaches obtaining a pair of communication bits, and translating the communication bits into three bit communication bits (column 6, lines 34-68, column 7, lines 1-24, and Figure 9). Kosaka1 teaches mapping the three bit communication bits into DQPSK symbols (columns 7-9,column 10 lines 1-29, and Figure 19).

Claims 22 is rejected under 35 U.S.C. 102(b) as being anticipated by Kosaka2 (US 5355092) (hereto referred to as Kosaka2). Kosaka2 teaches a method for demodulation of a communication signal, using DQPSK. Kosaka2 teaches obtaining Pi/4 DQPSK symbols and translating them into Quadrature phase shift keying (QPSK) symbols (column 2 lines 48-68, and Figure 4). Kosaka2 teaches mapping the QPSK symbols into a pair of bits (column 15 lines 58-68, column 16 lines 1-10, and Figures 6 and 22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosaka2, in view of Kosaka1.

As to claims 1, 10, and 15, Kosaka2 teaches a method and apparatus for demodulation of a communication signal, using DQPSK. Kosaka2 teaches obtaining Pi/4 DQPSK symbols and translating them into QPSK symbols (Kosaka2, column 2 lines 48-68, and Figure 4). Kosaka2 teaches mapping the QPSK symbols into a pair of bits (see Kosaka2, column 15 lines 58-68, column 16 lines 1-10, and Figures 6 and 22). Kosaka2 does not teach a method and apparatus for DQPSK modulation. Kosaka1 teaches a method and apparatus for modulation of a communication signal, using DQPSK. Kosaka1 teaches obtaining communication bits, and translating the

communication bits into three bits communication bits (Kosaka1, column 6, lines 34-68, column 7, lines 1-24, and Figure 9). Kosaka1 teaches mapping the three bits communication bits into DQPSK symbols (see Kosaka1, columns 7-9, column 10 lines 1-29, and Figure 19). It would have been obvious to one of ordinary skill in the art to combine the DQPSK demodulator of Kosaka2 with the DQPSK modulator of Kosaka1; a communication system must be capable of both receiving and transmitting a data signal. Therefore it would be obvious to one of ordinary skill in the art to combine the demodulator of Kosaka2, which is capable of receiving a signal, with the modulator of Kosaka1, which is capable of transmitting a signal, in order to create a functional communication system.

As to claims 2, 11, and 17, Kosaka2 does not teach translating two bits symbol into three bits symbol using XOR operation in DQPSK modulation. Kosaka1 teaches translating two bits symbol into three bits symbol using XOR operation in DQPSK modulation (see Kosaka1, column 6, lines' 34-68, column 7, lines 1-24 and Figure 9). It would be obvious to one of ordinary skill in the art to use an XOR operation in DQPSK modulation, because it is well known in the art that an XOR provides the correct translation needed to translate two bit symbol into a three bit symbol-using the minimum hardware and software requirements.

As to claims 5, 12, and 20, Kosaka2 teaches using a look up table to map the QPSK symbols into a pair of bits (see Kosaka2, column 15 lines 58-68, column 16 lines 1-10, and Figures 6 and 22).

As to claims 6 and 14, Kosaka2 teaches using a look up table to map the QPSK symbols into a pair of bits (see Kosaka2, column 15 lines 58-68, column 16 lines 1-10, and Figures 6 and 22).

As to claim 7, Kosaka2 does not teach translating two communication bits to three communication bits using XOR, ADDER, and other gate logic in DQPSK modulation. Kosaka1 teaches translating two communication bits to three communication bits using XOR, ADDER, and other gate logic in DQPSK modulation (see Kosaka1, column 6, lines 34-68, column 7, lines 1-24, and Figure 9). This translation as taught by Kosaka1 is functionally equivalent to providing two variable bits and a hardwired one bit to an adder, as claimed by the applicant in claim 7. It would be obvious to one of ordinary skill in the ad to use an XOR, ADDER, and other gate logic in DQPSK modulation, because it is well known in the art that an XOR, ADDER and other gate logic provide the correct translation needed to translate two bit symbol into a three bit symbol, using the minimum hardware and software requirements.

As to claim 8, Kosaka2 does not teach mapping the three bit communication bits into DQPSK symbols using a lookup table in DQPSK modulation. Kosaka1 teaches mapping the three bit communication bits into DQPSK symbols using a lookup table in DQPSK modulation (see Kosaka1, columns 7-9, column 10 lines 1-29, and Figure 19). It would be obvious to one of ordinary skill in the art to use a look up table, because it is well known in the art that a look up table can provide the correct translation needed to map the three bit communication bits into DQPSK symbols, using the minimum hardware and software requirements.

As to claims 9 and 16, Kosaka2 does not teach a method of modulation that does not require a complex multiplication operation. Kosaka1 teaches a method of modulation that does not require a complex multiplication operation. Kosaka1 teaches translating the communication bits to three communication bits using an XOR operation (see Kosaka1, column 6, lines 34-68, column 7, lines 1-24, and Figure 9), and teaches mapping the three bit communication bits into DQPSK symbols using a look up table (see Kosaka1, columns 7-9, column 10 lines 1-29, and Figure 19). These two steps of modulation as taught by Kosaka1 do not require a complex multiplication operation. It would be obvious to one of ordinary skill in the art to use an XOR operation and a look up table, because it is well known in the art that these elements can provide the correct translation and mapping needed in DQPSK modulation, using the minimum hardware and software requirements.

Claims 3, 4, 13, 18, and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Kosaka2 in view of Kosaka1 as applied to, respectively, claims 1, 10 and 15 above, and further in view of Dutta (US 5313493) (hereto referred to as Dutta).

As to claims 3, 13, and 18, Kosaka2 teaches a method for DQPSK demodulation. Kosaka2 does not teach the use of the formula claimed by the applicant in claim 3 in DQPSK demodulation. Dutta teaches translating the Pi/4 DQPSK symbols into QPSK symbols, using the formula $s'(t)=m(t)m(t-T)\exp[j\{\Delta wt-\Delta w(t-T)\}]$. Letting $s'(t)$ =SQPSK (t), $m(t)$ =S9T) and $T=1$, and using simple calculus, this formula can be equated to the formula claimed by the applicant in claim 3 (see Dutta, column 6 lines 41-45). It would have been obvious to one of ordinary skill in the art to use the formula taught by Dutta in

the demodulator taught by Kosaka2, so as to carry out the translation of Pi/4 DQPSK symbols into QPSK symbols.

As to claims 4 and 19, Kosaka2 teaches phase change calculation for demodulation (see Kosaka2, column 3 lines 43-64). This is functionally equivalent to claims 4 and 19 by the applicant.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
6-16-2005

KEVIN BURD
PRIMARY EXAMINER